192 GHz push–push VCO in 0.13 µm CMOS

C. Cao, E. Seok and K.K. O

A 192 GHz cross-coupled push–push voltage controlled oscillator (VCO) is fabricated using the UMC 0.13 µm CMOS logic process. The VCO can be tuned from 191.4 to 192.7 GHz. The VCO provides output power of ~−20 dBm and phase noise of ~−100 dBc/Hz at 10 MHz offset, while consuming 11 mA from a 1.5 V supply.

Introduction: With the rapid advance of high frequency capability for CMOS technology, millimetre-wave CMOS VCOs with ~100 GHz fundamental operating frequency have been reported [1, 2]. The fundamental oscillation frequency is limited by unity power gain frequency f_{max} of the transistor. To obtain even higher frequencies, push–push VCOs [3–5] using the second harmonic operating at up to 131 GHz have been demonstrated in a 90 nm CMOS technology [5]. In push–push VCOs, besides higher device gain, varactor and capacitor Q factors are higher, while the transmission line loss is lower at a given output frequency since the fundamental frequency of the oscillator is one half of the output frequency. In this Letter we report a 192 GHz push–push VCO fabricated using the 0.13 µm UMC logic process with eight copper layers. Oscillators such as this can be used in remote sensing and advanced imaging applications [6] and suggest that THz CMOS circuits will be available in the near future.

Circuit design: Fig. 1 shows the schematic of the VCO. Cross-coupled transistors M_1 and M_2 form the VCO core. Inductors, L_1 and L_2 (~45 pH), accumulation mode MOS capacitors, and the capacitances associated with M_1 and M_2 serve as the LC resonant tank. A key to achieving high fundamental operating frequency is minimising the parasitic capacitances connected to the LC tank [2]. At the virtual ground nodes, the anti-phase fundamental signals cancel out and the second-harmonic signal can be extracted. The middle point of inductors L_1 and L_2 has the lowest parasitic capacitance to ground among the common-mode nodes. This makes the impedance at resonant frequency the highest and the best port to extract the push–push output [3–5]. A quarter wavelength transmission line tuned for the second-harmonic frequency is usually used to increase the amplitude of the second harmonic while suppressing the fundamental signal [3–5]. In this design, the transmission line and the current source transistor are broken into two parts to make the layout symmetric, which better suppresses the fundamental signal at the common-mode nodes.

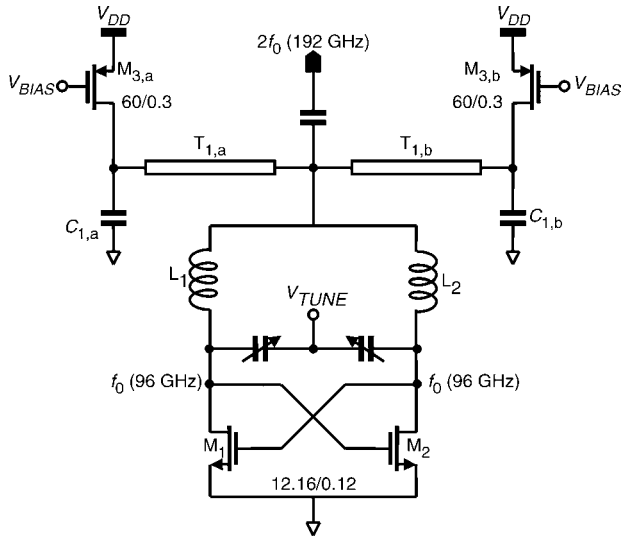

Fig. 1 *Schematic of push–push VCO*

The transmission line structure is shown in Fig. 2 and is formed using the grounded coplanar waveguide (CPW) structure [7, 8]. Compared to the conventional CPW, the ground plane isolates the line from the lossy silicon substrate and reduces the insertion loss. The lines are formed using the top metal (8) layer and the ground plane is formed by metal 1. The transmission line width and gap are 3 and 4 µm, respectively. The characteristic impedance of the line is ~65 Ω. The length of lines is 150 µm. This length is slightly shorter than $\lambda/4$, so that the impedance looking into the transmission line is inductive to resonate the capacitances from the pad and other metal interconnections. The 2 pF bypass capacitors ($C_{1,a}$, $C_{1,b}$ in Fig. 1) serve as a short around 190 GHz. They are formed using the parasitic capacitance between adjacent metal layers [9]. The metal 8, 6, 4 and 2 layers form the top plate, and metal 7, 5, 3 and 1 layers form the bottom plate. The capacitance density is 0.55 fF/µm^2. The transmission lines and bypass capacitors are simulated using the Ansoft HFSS, a 3D EM simulator. Two VCOs are implemented. In the first version, to achieve higher oscillation frequency, the output buffers and bond pads for the fundamental output were not included. The chip occupies 450 × 390 µm including the bond pads. A micrograph is shown in Fig. 3. The second VCO, including the buffers for both the fundamental and push–push port, was also fabricated. Owing to the capacitance from output buffer, the measured fundamental oscillation frequency is about 4 GHz lower.

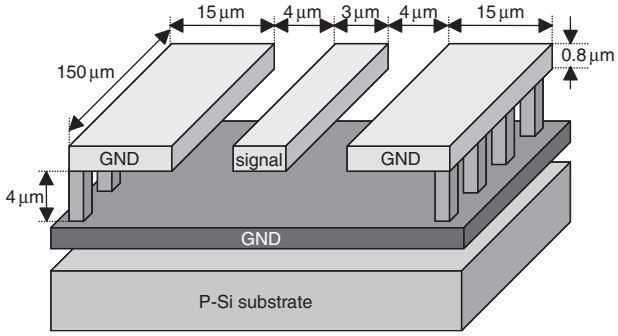

Fig. 2 *Grounded coplanar waveguide transmission line*

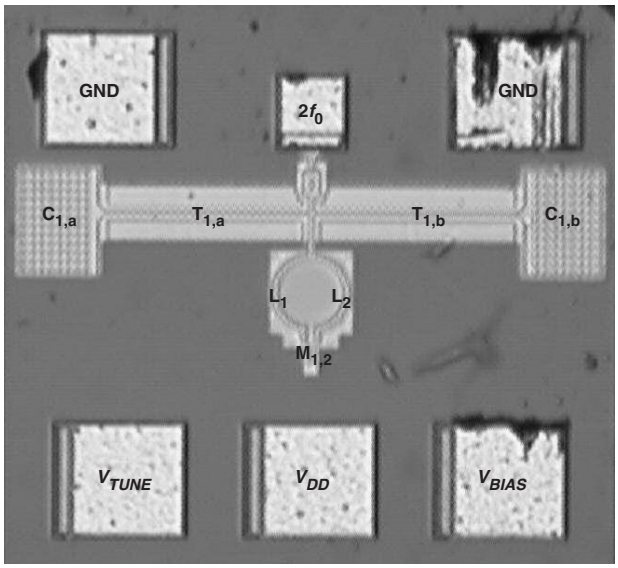

Fig. 3 *Micrograph of chip*

Experiment results: The chip was measured on-wafer using a GGB WR-5 (140–220 GHz) waveguide probe. The cutoff frequency of the TE_{10} mode in the WR-5 waveguide is 115.7 GHz, which attenuates the fundamental signal entering the harmonic mixer. The VCO output spectrum is measured using an OML M05HWD (140–220 GHz) harmonic mixer and an Agilent E4448A 50 GHz spectrum analyser. An Agilent 11970W (75–110 GHz) harmonic mixer has also been used to evaluate the fundamental output.

The circuit starts to oscillate with 3.2 mA current. However, no signal was detected at the push–push port until the bias current is increased to above 8 mA owing to the detection limit of the measurement setup. To increase the output level, the circuit is measured with 11 mA bias current from a 1.5 V supply. Fig. 4 shows the output spectrum and the measured signal level is −82 dBm. The conversion loss of the harmonic mixer is ~60 dB at 190 GHz. The insertion loss of the probe is about 2 dB. Thus, the signal is estimated to be about −20 dBm. The oscillation frequency can be tuned from 191.4 to 192.7 GHz by

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changing V_{TUNE} from 0 to 1.8 V. Because the output of harmonic mixer is weak, the phase noise could not be directly measured. The phase noise of the fundamental output is −106 dBc/Hz at 10 MHz offset for the VCO with the output buffer. The phase noise at the push–push port is expected to be 6 dB higher. Owing to the coupling through the substrate and metal interconnection, the fundamental signal also appears at the push–push port. The measured fundamental signal is about −30 to −25 dBm at the push–push port after calibrating the losses. As expected, the frequency range of the fundamental signal is exactly one half of the second harmonic.

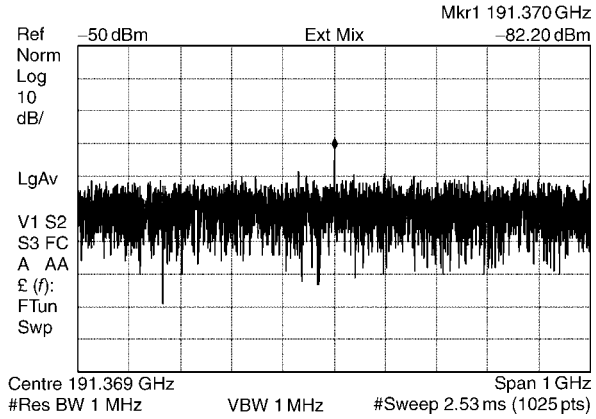

Fig. 4 *Measured VCO output spectrum*

Conclusions: A 192 GHz push–push VCO fabricated in the UMC 0.13 µm CMOS process is presented. 192 GHz is the highest operating frequency for any silicon-based circuits. Given that the state of the art is 65 nm, generation of THz signals using CMOS technology cannot be far in the future.

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